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PH. DOCTOR

MICROELECTRONICS COMPUTING

Graduated from a French engineering school in 2008 and owner of a Ph.D. in microelectronics since December 2012, I am looking for a position in research and development which match with my capabilities and skills (not necessarily in the field of microelectronics).

EDUCATION

Ph.D. in Microelectronics — *March 2009 – December 2012*

Within Cadence Design System, a well-known company in the field of EDA (electronic design automation), I realized a thesis with the IM2NP laboratory. I got my PhD with **Class Honours**. My subject was "Current Driven Layout Generation for Full Custom Design" and my goal was to develop solutions for the consideration of currents constraints during routing phase for strong currents analog blocks. Some details of my work are given in the section "Professional Experience" below.

Engineering School ISEN-Toulon — *September 2003 – September 2008*

ISEN (*Institut Supérieur de l'Electronique et du Numérique*) is a general engineering school with integrated preparatory classes, which is recognized by the **CTI** (*Commision des Titres d'Ingénieur*). I was **major of promotion** both in first and third year. My options choices were generally oriented towards microelectronics, with a specialization in the last year.

Master M2 MINELEC Microelectronics Research — *September 2007 – August 2008*

My last year specialization at ISEN allowed me to get a double degree with the Aix-Marseille University of Provence. I passed second of the promotion with 14.78/20 points.

PROFESSIONAL EXPERIENCE

Ph.D. in Microelectronics — *March 2009 – December 2012*

Cadence Design System / IM2NP — **Sophia-Antipolis / Marseille (France)**

In deep submicron VLSI circuits, excessive current density in interconnects is a major concern for analog high current application. If current over maximum density is not effectively mitigated, this can lead to phenomena like electromigration, voltage drop and electrical overload. It is a hot topic of interest in modern circuits due to the decrease of metal track sizes while high currents are necessary in automotive or mobile applications. This thesis had as goal to develop solutions for the consideration of the constraints in the current phase of routing analog blocks strong currents.

This work had for objective the **development of solutions** for current constraints considerations during **routing phase** for strong currents analog blocks. Firstly, after a phase of bibliography to learn about the state of the art, I studied the tools at my disposal (being directly at Cadence, I had access to their tools easily). I then developed analytical functions (in Skill). A method for characterizing the currents has been defined, a good knowledge of the currents in

interconnexions being essential. Current data extraction functions were made by running (using **Skill and Ocean** languages, which are specific to Cadence tools).

An **algorithmic approach** for guided routing was then initiated. An exhaustive routing algorithm has been developed (in Skill at first, in **C++** subsequently, using **OpenAccess libraries** to interact with Cadence tools) and then used to search good topology criteria. Two algorithms were then studied and compared, an existing greedy algorithm used as a reference, and an original one, called "Divide & Conquer". This algorithm, also developed in C++, generates an **optimized routing** for a minimum interconnects area while respecting minimum widths in order to show no violation of current density. It shows results improved on average by about 10% for area and almost 27% for CPU time compared with existing solution. This work resulted in **three publications** in conferences (SAME 2009, SAME 2010 and SMACD 2012).

Another part of my work focused an automatic method to avoid issues due to current crowding in corner bends, with a method based on a set of **mathematical models**. These models are used to determine the optimized surface for support shapes in corner bends, to decrease current crowding effects with a minimal increase in interconnections area . The models were generated by using **design of experiment** methods, with the help of a current solver (macros helped to automate these steps). A C++ function identifies corners bends in the layout and automatically apply the support shapes. This work resulted in **one publication** (DCIS 2012).

During this PhD, I coached for two consecutive years a Digital Design course (creation of a microcontroller using VHDL).

End of studies internship (MFE) *February to August 2008 (6 months)*

ATMEL, Digital Libraries Service **Rousset (France)**

The subject of this internship was the implementation of an eDFM flow (electrical Design For Manufacturing) for advanced technologies (90nm and below). The effects which have been implemented in the design flow are Well Proximity Effect (WPE) and Shallow Trench Isolation effect (STI effect).

After some bibliographic research, I developed simulations functions to see the impact of these effects in Skill and Ocean. From the very initial results, it turned out that the STI effect had a significant impact, then it would be very useful to insert it into the flow. To take into account this effect, it was necessary to define new layers, edit the transistor cells in libraries to add some parameters and modify extraction files (Assura).

Besides the work on eDFM and STI effect, modeling algorithms for Gate Bending (transistors with gates at 45°) were studied. After an initial phase of bibliographic research, a test cell was created to check the models accuracy.

Application Engineer Internship (SAI) *June to September 2007 (4 months)*

ATMEL, Physical Design Kit Group **Rousset (France)**

The subject of this internship was the implementation of a design flow for the analysis of substrate coupling (also called substrate noise). First, the software for the analysis has been installed and configured for the PDK design flow. An evaluation of the software was then performed, compared to well-known data regarding the influence on the noise of protections such as Guard Ring and Deep Nwell. Finally, the tool limitations in terms of cell size were highlighted by the use on a complex cell, which helped to define a rule: limit the analysis to sensitive areas, by using a layer to delimit these areas.

Besides the main activity, I worked at the realization of procedures for the design kit qualification flow. Two functions have been developed using Skill and Ocean languages, both integrated into the qualification flow. These functions tested the cell compatibility of various libraries with a new version of the Cadence software.

Worker internship *July-August 2005 (2 months)*

CNIM **La Seyne-sur-Mer (France)**

The purpose of this internship was to familiarize me with the industrial production conditions. Within the pedestrians' transportation department, I participated in the production line of escalators and moving sidewalks.

Seasonal employment — *Summers 2003, 2004 and 2006*

Crédit Agricole (Bank) — **Hyères (France)**

I worked several summers as a bank auxiliary, holding the wicket to serve customers, managing back-office, handling telephone calls.

SKILLS

My activities were mostly oriented on **research and development**, mainly in microelectronics computing (EDA). I worked extensively on the tools used for electronic design.

Electronics / Microelectronics

From my experiences, I have learned to know the design tools (Cadence). I developed several functions which were integrated into these tools (using Skill, a language derived from Lisp and used by Cadence, and **C++** with OpenAccess libraries). I know the Full-Custom flow, and have a good knowledge of current constraints.

I also have knowledge in: Analog Design, Digital Design, Components Modeling, Digital Architecture, RF Architecture, IC Testing, CMOS Reliability, Memories

Other areas

In addition to the subjects studied during my schooling (Telecoms, Network and Systems, Management, Object Oriented Programming), I am also self-taught Web Design (static and dynamic) and Graphical Design.

Known Programming Languages

Skill et Ocean (langages Cadence), **C++**, VHDL, Shell, Assembly language, C, PHP, Javascript, HTML, XML, SQL, VBA

Known Softwares

CADENCE (ICFB, ADE, Assura, Virtuoso, NCLaunch), Calibre, CST EM Studio, Statsoft Statistica, Matlab, Mapple, Protel DXP, Photoshop, Illustrator, Dreamweaver, Flash, MS Suite

Languages

English: First Certificate of Cambridge (obtained in 2004), C grade, TOEIC equivalent between 750 and 825 points).
French: Native language

ADDITIONAL INFORMATION

Associative activities

Although these are not literally professional experiences, associative activities in my school brought their part of experiences, and therefore deserve to be mentioned. During my studies, I was part of the organization committee for the “Forum des Métiers” in 2007 (a meeting forum between students and companies). I was a member of the *ISEN Espérance*, the humanitarian organization of the school, which oversees various projects.

Outside the school context, I was a volunteer with the association “*Voir Ensemble*”, which helps the integration of visually impaired people in Toulon for one year.

Passions and Interests

I have a particular passion for creating websites, both in terms of design (graphics and layout) and programming (static and dynamic). Another passion, reading. I love Fantasy and Science Fiction novels, which allow to escape and develop the imagination, but I do not limit myself to these genres. Another activity that combines two of my passions, the RPG

forums, a kind of multi author role play writing, on an online support. I'm also a big fan of RPG videogames (including Final Fantasy for example).

I do some sport like Roller and Vo Dao (Vietnamese martial arts), not to mention skiing in winter. I also like to travel: Spain, Italy, the United States (California, Florida), particularly Canada, a beautiful country. I love History, visiting monuments, museums (big fan of the Louvre, where I could forget myself for days...), walks in the forest, by the sea...

Qualities

Adaptability, reliability, responsibility, creative, curious, conscientious, analytical, methodical.

Driver License

I have a French driving license.